REMARKS

Claims 21-23, 25, 65, 67, 68, 70 and 71 are amended. Claims 24, 26, 27, 64, 66, 69, 72 and 73 are canceled. Claims 21-23, 25, 28, 65, 67, 68, 70, 71, 74 and 75 are in the application for consideration.

Independent claim 21 stands rejected as being obvious over a combination of Tsu et al. and Miller et al. Claim 21 is directed to DRAM circuitry comprising an array of word lines and a plurality of memory cell storage capacitors, where the capacitor dielectric region within individual memory cell storage capacitors comprises aluminum nitride with the region contacting the first and second capacitor electrodes and having a thickness which is less than or equal to 60 Angstroms.

Miller et al. is relied upon as disclosing an impedance matching capacitor having an AlN comprising capacitor dielectric region 12. However, it would not be obvious, nor would a person look to Miller et al., to arrive at Applicant's claim 21 invention. Miller et al. is directed to forming a shunt capacitor, which is a passive capacitor element utilized for impedance matching (*see*, for example, col.2, lns.30-41). The impedance matching dielectric is some 380 microns in thickness, and extends the length of a fully encapsulated chip to facilitate each individual active element of the whole chip having the same electrical load (col.2, lns.20-26 and lns.41-45). Such is not even remotely related to or an applicable teaching to Applicant's DRAM circuitry fabrication of a magnitude of 60 Angstroms or less. Indeed, the 380 microns thickness of Miller et al. equates to 3,800,000 Angstroms, which is some 63,000+ times greater than the scale of

Applicant's claimed circuitry devices. Specifically, Applicant's field of endeavor is directed to the fabrication of active capacitors in DRAM circuitry at a very small scale, not directed to the fabrication of passive capacitors beyond chip level at more than 63,000 times the size of Applicant's capacitor dielectric layer. Further, the use of a dielectric region 12 in Miller et al. is not in any way associated with the fabrication of any memory circuitry. *See*, for example, *Wang Laboratories, Inc. v. Toshiba Corp.*, 993 F.2d 858; 26 U.S.P.Q.2d 1767 (Fed. Cir. 1993), where even patent claims and an art reference both directed to memory modules still resulted in a conclusion that the art was non-analogous. Here, where Miller et al. doesn't even relate to memory circuitry and is of a vastly different fabrication scale, the art is clearly non-analogous.

Accordingly, it is respectfully asserted that one would not combine Miller et al. with Tsu et al., both due to their respective arts being non-analogous with one another, and as well there simply being no teaching in any of the cited art of using aluminum nitride as at least part of the capacitor dielectric region in DRAM memory circuitry. The Examiner asserts that it would be obvious to modify Tsu et al. to form a capacitor dielectric layer of AlN to reduce carbon and oxygen incorporation in order to prevent current leakage. However, there is no reference in either Miller et al. or Tsu et al. with respect to such, with the Examiner only asserting the alleged motivation to modify by looking at Applicant's specification.

For the foregoing reasons, the rejection of Applicant's independent claim 21 over Tsu et al. and Miller et al. should be withdrawn, and action to that end is requested.

Applicant's dependent claims should be allowed as depending from allowable base claims, and for their own recited features which are neither shown nor suggested in the cited art. For example, with respect to claim 23, such stands rejected further in view of Dornfest et al. The Examiner asserts that Dornfest et al. discloses a native oxide formed on at least one of first and second capacitor electrodes 44 and 36. However, the undersigned has reviewed the Dornfest et al. reference and finds no such indication. Indeed, col.4, lns.48-54 and col.8, lns.36-40 specifically teach not forming any native oxide. Thus, the reference teaches away from that which Applicant recites in claim 23. Accordingly, the obviousness rejection thereof should be withdrawn. Further, the Examiner persists in referring to cols.34-49 in the Dornfest et al. reference. The patent only has 12 columns, so the undersigned is left guessing as to what the Examiner is referring. If the Examiner is to persist in this rejection, it is requested that the Examiner remove reference to cols.34-49, and specifically identify where the Examiner's assertions are supported.

The undersigned appreciates the Examiner's review and initialing of the prior art listed on a Form PTO-1449 submitted in a Supplemental Disclosure Statement (SIDS) signed and filed on May 29, 2003. However, the undersigned also submitted two other SIDS's signed and filed on December 30, 2002 and August 27, 2003, respectively, but no initialed Forms PTO-1449 were included in

the last Office Action. Duplicate copies of the two uninitialed Forms PTO-1449 are attached. In addition, another SIDS is submitted herewith.

This application is believed to be in immediate condition for allowance, and action to that end is requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 11-20-03

By: _____
Mark S. Matkin
Reg. No. 32,268